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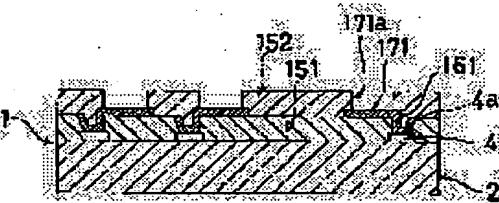
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## (54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

### (57)Abstract:

**PURPOSE:** To provide the semiconductor device, which can be manufactured as the high-quality product in excellent productivity even if the number of semiconductor elements becomes many, the electrodes of the semiconductor elements are made small and the electrode pitch is narrowed.

**CONSTITUTION:** This device has the following parts. A semiconductor element 2 has a plurality of element electrodes 4, wherein integrated circuits are formed. A first insulating layer 151 is formed on the surface of the semiconductor element 2. A plurality of external electrodes 171 are formed on the first insulating layer 151. A first wiring part 161 connects the external electrode 171 and the element electrodes 4 electrically. The first conductive layers comprising these parts are provided.



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CLAIMS

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[Claim(s)]

[Claim 1] The semiconductor device characterized by having the 1st conductive layer which consists of the 1st wiring which connects electrically two or more external electrodes formed on the semiconductor device which an integrated circuit is formed and has two or more component electrodes, the 1st insulating layer formed in the front face of said semiconductor device, and said 1st insulating layer, and said external electrode and said component electrode.

[Claim 2] The semiconductor device which an integrated circuit is formed and has two or more component electrodes, and the 1st insulating layer formed in the front face of said semiconductor device, The 1st conductive layer which consists of the 1st wiring which was formed on said 1st insulating layer and was electrically connected with said component electrode, The semiconductor device characterized by having the 2nd conductive layer which consists of the 2nd wiring which connects electrically the 2nd insulating layer formed on said 1st conductive layer, two or more external electrodes formed on said 2nd insulating layer, and said external electrode and said 1st wiring, or said component electrode.

[Claim 3] The semiconductor device according to claim 2 with which the external electrode which has the multilayer-interconnection structure where the insulating layer and the conductive layer were repeatedly formed on the surface of the semiconductor device, and was electrically connected with the component electrode of said semiconductor device through said multilayer-interconnection structure is formed in the maximum front face.

[Claim 4] The coefficient of thermal expansion of the insulating material of an insulating layer is a semiconductor device according to claim 1, 2, or 3 which is the middle value of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board.

[Claim 5] The insulating material of an insulating layer is a semiconductor device according to claim 1, 2, 3, or 4 which is a photosensitive epoxy resin.

[Claim 6] Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, The manufacture approach of the semiconductor device characterized by having the 1st conductive layer formation process which prepares the 1st conductive layer which consists of the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and connects electrically an external electrode, and two or more of said external electrodes and said component electrodes.

[Claim 7] Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, The 1st conductive layer formation process which prepares the 1st conductive layer which has the 1st wiring

which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and is connected to said component electrode, Form the insulating layer by the photosensitive insulating material on said 1st conductive layer, and negatives are exposed and developed using a mask. The 2nd insulation layer forming process which prepares the 2nd insulating layer which has a through tube to said 1st wiring, The conductive layer by the conductive ingredient is formed on said 2nd insulating layer, and it operates orthopedically. Two or more external electrodes, The manufacture approach of the semiconductor device characterized by having the 2nd conductive layer formation process which prepares the 2nd conductive layer which consists of the 2nd wiring which connects electrically said external electrode and said 1st wiring, or said component electrode.

[Claim 8] The manufacture approach of a semiconductor device according to claim 7 of repeating an insulation layer forming process and a conductive layer formation process on the surface of a semiconductor device, establishing multilayer-interconnection structure, and preparing the external electrode electrically connected with the component electrode of a semiconductor device through said multilayer-interconnection structure in the maximum front face.

[Claim 9] The manufacture approach of a semiconductor device according to claim 6, 7, or 8 of giving an insulation layer forming process and a conductive layer formation process to two or more semiconductor devices of the condition of a wafer.

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**DETAILED DESCRIPTION**

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the semiconductor device which mounted the semiconductor device in high density at the semi-conductor carrier, and its manufacture approach.

[0002]

[Description of the Prior Art] The conventional semiconductor device mounted in high density is explained to the circuit board based on drawing 5 – drawing 8.

[0003] It has connected with the circuit board 12, once connecting with the semi-conductor carrier 3 and using a semiconductor device 2 as a semiconductor device 1 from the former, as shown in drawing 6 when it mounts a semiconductor device 2 in the circuit board 12. There are the following two reasons in this.

[0004] With a raise in basic wages semiconductor device, a blemish tends to be attached and inspection of the 1st reason is impossible before mounting. Therefore, in order to enable it to inspect before mounting and to prevent property degradation by humidity, the semi-conductor carrier 3 is equipped with a semiconductor device 2, and restoration covering of the circumference is carried out with the encapsulant 7 of epoxy system resin.

[0005] As for the 2nd reason, a bias tooth space is constitutionally restricted for a component electrode location to the periphery of a raise in basic wages semiconductor device, these component electrodes 4 with which the tooth space was restricted are small, and, as for a raise in basic wages semiconductor device, its inter-electrode distance is narrow. Therefore, it is difficult to connect said component electrode 4 to the substrate electrode 11 of the circuit board 12 directly.

[0006] In order to make this connection easy, arrangement of the component lateral electrode 6 of one side is suitable for connection with the component electrode 4 of a semiconductor device 2, and arrangement of the substrate lateral electrode 8 of an opposite side connects a semiconductor device 2 to said one side of the semi-conductor carrier 3 suitable for connection with the substrate electrode 11 of the circuit board 12, and is carrying out restoration covering of that circumference with the encapsulant 7 of epoxy system resin by the aforementioned reason.

[0007] Therefore, in the 1st conventional example, in drawing 6, a semiconductor device 1 forms the golden bump 5 on it, connects the component electrode 4 of a semiconductor device 2 to the component lateral electrode 6 of the semi-conductor carrier 3 with cream solder or electroconductive glue, and carries out restoration covering of the clearance between the connected semiconductor device 2 and the semi-conductor carrier 3, and the connected periphery of a semiconductor device 2 with the encapsulant 7 of epoxy system resin. And it connects electrically between said component lateral electrodes 6 and said substrate lateral electrodes 8.

[0008] In connecting a semiconductor device 1 to the circuit board 12, as first shown in drawing 6, a bump 9 is formed in said substrate lateral electrode 8 of the semi-conductor carrier 3, and it prints the cream solder 13 to the substrate electrode 11 of the circuit board 12.

[0009] Subsequently, as shown in drawing 7, the substrate lateral electrode 8 of a semiconductor device 1 is positioned, laid and heated on the substrate electrode 11 of the circuit board 12, melting and hardening of said applied cream solder 13 are done, and the substrate lateral electrode 8 is connected to the substrate electrode 11.

[0010] Next, the 2nd conventional example is explained based on drawing 8.

[0011] In drawing 8, a semiconductor device 1 forms the golden bump 5 on two or more component electrodes 4 of a semiconductor device 2, and connects the bump 5 of said gold to the component lateral electrode 6 formed on the polyimide film 14 of electroconductive glue 5a, and the gap of a semiconductor device 2 and a polyimide film 14 is filled up with the encapsulant 7 of epoxy system resin. And a bump 9 is formed in the component lateral electrode 6, and this is connected to the electrode of the circuit board. Although drawing 8 shows a cross section, in fact, it is arranged at space perpendicularly densely [ the component electrode 4 of a large number which incline toward the periphery of a semiconductor device 2 ], and the component lateral electrode 6 is arranged in the shape of a grid to the tooth space where the center section of the semiconductor device 2 is large.

[0012]

[Problem(s) to be Solved by the Invention] However, as shown in drawing 5, a process until it ships as a semiconductor device from the wafer of a semiconductor device needs to divide the wafer of a semiconductor device into each semiconductor device at a division process, and needs to repeat bump formation of only the number of the component electrodes to each semiconductor device with a bump formation process, and it is necessary to do positioning and junction of the semiconductor devices which bump formation ended at positioning / junction process one by one with the configuration of the above-mentioned conventional example, at a semi-conductor carrier.

[0013] Therefore, when the number of the component electrodes of a semiconductor device increases like recently, there is a trouble that a production process takes time amount very much.

[0014] Moreover, there is a trouble that the hardening process of the encapsulant 7 shown in drawing 6 and drawing 7 also takes a long time.

[0015] As a property for which the semi-conductor carrier 3 is asked, moreover, the display flatness In order to maintain the dependability of electrode bonding strength, the amount of curvatures of the

magnitude of 10 micrometers or less and a substrate lateral electrode is more than 100micrometerx100micrometer. If the amount of curvatures exceeds 10 micrometers, poor electrode junction will occur, and if the area of a substrate lateral electrode runs short or a pitch becomes narrow too much, manufacture of high quality will become difficult, and there is a trouble that the defect of a bridge etc. occurs.

[0016] This invention makes it a technical problem to offer the semiconductor device which can manufacture the product of high quality with sufficient productivity, and its manufacture approach, even if solve the above-mentioned trouble, the number of component electrodes of a semiconductor device increases, the component electrode of a semiconductor device becomes small and an electrode pitch becomes narrow.

[0017]

[Means for Solving the Problem] The semiconductor device of the 1st invention of this application is characterized by having the 1st conductive layer which consists of the 1st wiring which connects electrically two or more external electrodes formed on the semiconductor device which an integrated circuit is formed and has two or more component electrodes, the 1st insulating layer formed in the front face of said semiconductor device, and said 1st insulating layer, and said external electrode and said component electrode, in order to solve the above-mentioned technical problem.

[0018] The semiconductor device which an integrated circuit is formed and has two or more component electrodes in order that the semiconductor device of the 2nd invention of this application may solve the above-mentioned technical problem, The 1st insulating layer formed in the front face of said semiconductor device, and the 1st conductive layer which consists of the 1st wiring which was formed on said 1st insulating layer and was electrically connected with said component electrode, It is characterized by having the 2nd conductive layer which consists of the 2nd wiring which connects electrically the 2nd insulating layer formed on said 1st conductive layer, two or more external electrodes formed on said 2nd insulating layer, and said external electrode and said 1st wiring, or said component electrode.

[0019] Moreover, in order to solve the above-mentioned technical problem, it is suitable for the semiconductor device of the 2nd invention of this application that the external electrode which has the multilayer-interconnection structure where the insulating layer and the conductive layer were repeatedly formed on the surface of the semiconductor device, and was electrically connected with the component electrode of said semiconductor device through said multilayer-interconnection structure is formed in the maximum front face.

[0020] Moreover, in order that the semiconductor device of the 1st, 2nd, or 3rd invention of this application may solve the above-mentioned technical problem, it is suitable for the coefficient of thermal expansion of the insulating material of an insulating layer that it is the middle value of the coefficient of thermal expansion of a semiconductor device and the coefficient of thermal expansion of the circuit board.

[0021] Moreover, in order to solve the above-mentioned technical problem, as for the semiconductor device of the 1st, 2nd, 3rd, or 4th invention of this application, it is suitable for the insulating material of an insulating layer that it is a photosensitive epoxy resin.

[0022] In order that the manufacture approach of the semiconductor device the 3rd invention of this application may solve the above-mentioned technical problem Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, It is characterized by having the 1st conductive layer formation process which prepares the 1st conductive layer which consists of the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and connects electrically an external electrode, and two or more of said external electrodes and said

component electrodes.

[0023] In order that the manufacture approach of the semiconductor device the 4th invention of this application may solve the above-mentioned technical problem Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, The 1st conductive layer formation process which prepares the 1st conductive layer which has the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and is connected to said component electrode, Form the insulating layer by the photosensitive insulating material on said 1st conductive layer, and negatives are exposed and developed using a mask. The 2nd insulation layer forming process which prepares the 2nd insulating layer which has a through tube to said 1st wiring, It is characterized by having the 2nd conductive layer formation process which prepares the 2nd conductive layer which consists of the 2nd wiring which forms the conductive layer by the conductive ingredient on said 2nd insulating layer, operates orthopedically, and connects electrically two or more external electrodes, and said external electrode and said 1st wiring, or said component electrode.

[0024] Moreover, in order to solve the above-mentioned technical problem, it is suitable for the manufacture approach of the semiconductor device the 4th invention of this application to repeat an insulation layer forming process and a conductive layer formation process on the surface of a semiconductor device, to establish multilayer-interconnection structure, and to prepare the external electrode electrically connected with the component electrode of a semiconductor device through said multilayer-interconnection structure on the maximum front face.

[0025] Moreover, in order to solve the above-mentioned technical problem, it is suitable for the manufacture approach of the semiconductor device the 3rd or 4th invention of this application to two or more semiconductor devices of the condition of a wafer to give an insulation layer forming process and a conductive layer formation process.

[0026]

[Function] The manufacture approach of the semiconductor device of the invention in this application, and the semiconductor device of the invention in this application Form the insulating layer by the photosensitive insulating material in the front face of the semiconductor device which an integrated circuit is formed and has two or more component electrodes, and negatives are exposed and developed using a mask. The 1st insulation layer forming process which prepares the 1st insulating layer which has a through tube to said component electrode, It is what is depended on combination with the 1st conductive layer formation process which prepares the 1st conductive layer which has the 1st wiring which forms the conductive layer by the conductive ingredient on said 1st insulating layer, operates orthopedically, and is connected to said component electrode. Since these processes can use the track record of the manufacturing technology of a semiconductor device, a quality semiconductor device can be obtained corresponding to the component electrode of the semiconductor device made [ overly ] detailed, or its pitch.

[0027] Moreover, since the process of the conventional technique which requires the time amount of attaching a-bump-for-every-component electrode of a semiconductor device is lost, it bundles up for every semiconductor device, it bundles up for every wafer further and a component electrode and external inter-electrode electrode junction is performed, productivity can be improved very greatly.

[0028] Moreover, by using the insulating material which has the middle coefficient of thermal expansion of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board in the insulating material to be used, the thermal stress generated according to the difference of thermal expansion is eased, and dependability can be improved.

[0029]

[Example] The 1st example of the semiconductor device of this invention is explained based on drawing

1 and drawing 2 R> 2.

[0030] In drawing 1 and drawing 2 , the 1st insulating layer 151 is formed on the semiconductor device 2 in which the structure of the semiconductor device 1 of this example has two or more component electrodes 4, and through tube 4a is prepared on the component electrode 4. On the 1st insulating layer 151, the 1st wiring 161 and the 1st external electrode 171 were formed, and the 1st wiring 161 has connected the 1st external electrode 171 and the component electrode 4. The 2nd insulating layer 152 was formed on the 1st insulating layer 151, the 1st wiring 161, and the 1st external electrode 171, and through tube 171a has opened on the 1st external electrode 171. This 1st external electrode 171 turns into an external electrode of the semiconductor device 1 of this example.

[0031] And although the area of the component electrode 4 will become small and an inter-electrode pitch will become narrow if a semiconductor device 2 is miniaturized and the number of the component electrodes 4 increases since it inclines toward the periphery of a semiconductor device 2 and is arranged by the configuration of a semiconductor device 2 as the component electrode 4 is shown in drawing 2 The 1st external electrode 171 is arranged to the tooth space where the center section of the semiconductor device 2 is large, there are few limits of a form, area, and arrangement, and as shown in drawing 2 , it can be freely designed to the arrangement which is easy to connect to the substrate electrode of the circuit board at arrangement of the shape for example, of a grid etc.

[0032] The 2nd example of the semiconductor device of this invention is explained based on drawing 3 .

[0033] In drawing 3 , the structure of semiconductor device 1a of this example makes structure of the 1st example multilayer structure.

[0034] The 1st insulating layer 151 is formed on the semiconductor device 2 which has two or more component electrodes 4, and through tube 4a is prepared on the component electrode 4.

[0035] On the 1st insulating layer 151, the 1st wiring 161 and 1st connection electrode 161a were prepared, and the 1st wiring 161 is connected to the component electrode 4 and 1st connection electrode 161a.

[0036] The 2nd insulating layer 152 is formed on the 1st insulating layer 151, the 1st wiring 161, and 1st connection electrode 161a, and through tube 161b is prepared on 1st connection electrode 161a.

[0037] On the 2nd insulating layer 152, the 2nd wiring 162 and the 2nd external electrode 172 were formed, and the 2nd wiring 162 is connected to 1st connection electrode 161a.

[0038] The 3rd insulating layer 153 is formed on the 2nd insulating layer 152, the 2nd wiring 162, and the 2nd external electrode 172, and through tube 172a is prepared on the 2nd external electrode 172.

[0039] The above-mentioned multilayer structure is possible and can design any number of layers [ not only two-layer but ] addition of circuit elements, such as resistance and capacity, in the wiring section of these layers.

[0040] The manufacture approach of the semiconductor device of this invention is explained based on drawing 4 and drawing 5 R> 5.

[0041] In drawing 4 , 1st insulating-layer 151a is first formed in the front face of the semiconductor device 2 which has the component electrode 4 with the 1st insulation layer forming process by the photosensitive insulating material. As for a photosensitive insulating material, it is desirable that it is epoxy system resin. Formation of 1st insulating-layer 151a may print a liquefied thing, and may make a film-like thing adhere.

[0042] Next, it takes exposure 18 at an exposure process using the mask 17 formed so that the light of a predetermined pattern might pass.

[0043] Next, at a development process, by developing negatives, through tube 4a is prepared on the component electrode 4, and the 1st insulating layer 151 is formed.

[0044] Next, 1st conductive ingredient layer 171c is formed with the 1st conductive ingredient layer formation process on the 1st aforementioned insulating layer 151, through tube 4a, and the component electrode 4. If a thin film can be formed and a fine pattern can be formed, various kinds of processing approaches, such as plating, sputtering, and vacuum evaporationo, can be freely chosen as formation of

this 1st conductive ingredient layer 171c.

[0045] Next, at a plastic surgery process, from said 1st conductivity ingredient layer 171c, it etches by leaving a required part and the 1st wiring 161 and the external electrode 171 are formed. Of course, the plastic surgery approach can also be chosen freely.

[0046] Next, 2nd insulating-layer 152a is formed in the front face of the 1st insulating layer 151, the 1st wiring 161, and the external electrode 171 by the photosensitive insulating material with the 2nd insulation layer forming process. As for a photosensitive insulating material, it is desirable that it is epoxy system resin. Formation of 2nd insulating-layer 151a may print a liquefied thing, and may make a film-like thing adhere.

[0047] Next, at exposure / development process, it exposes, and by developing negatives, through tube 171a is prepared on the external electrode 171, and the 2nd insulating layer 152 is formed.

[0048] In drawing 4, although it seems that mutual spacing of two or more external electrodes 171 is narrow, as shown in drawing 2, it is arrangement of the shape of a grid which is perpendicularly separated in space in fact.

[0049] Depending on the case, even the n-th wiring layer formation process and the n-th insulation layer forming process are repeatedly made into multilayer structure. In that case, components, such as resistance and capacity, can be added to each wiring layer. And the insulating material used above has a desirable ingredient with the middle coefficient of thermal expansion of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board, as shown in Table 1.

[0050]

[Table 1]

素材	熱膨張係数 ( $10^{-6}$ / °C)
半導体素子	2.4
絶縁層	3~6
回路基板 (アルミナ基板)	7

[0051] In addition, although it is drawing which performs a wiring layer formation process and an insulation layer forming process after dividing a semiconductor device wafer in drawing 4 used for explanation of an example, since the semiconductor device of the whole wafer is put in block and the n-th wiring layer formation process and the n-th insulation layer forming process can be processed in the condition before division of a semiconductor device wafer, working efficiency improves very greatly.

[0052] Moreover, since a wiring layer formation process and an insulation layer forming process are the repeats of the production process of a semiconductor device, and the same process, and the thing equivalent to the manufacture track record of a semiconductor device is possible for such process tolerance, corresponding to the electrode made [overly] detailed or its pitch, manufacture of the semiconductor device of high quality is possible for it.

[0053] The process of this invention and the conventional example is compared based on drawing 5.

[0054] In drawing 5, although the right-hand side conventional example is as explanation of the above In the case of left-hand side this invention, the n-th wiring layer formation process and the n-th insulation layer forming process in the condition before division of a semiconductor device wafer Since the semiconductor device of the whole wafer can be processed collectively, after dividing a semiconductor device wafer, as compared with forming a bump, working efficiency improves extremely for every electrodes of those for every sheet of every of a semiconductor device in the conventional example.

[0055]

[Effect of the Invention] By the semiconductor device and its manufacture approach of this invention, since a wiring layer formation process and an insulation layer forming process are both the repeats of

the production process of a semiconductor device, and the same process, it can respond to the electrode of the semiconductor device made [ overly ] detailed, or its pitch, and the effectiveness that the semiconductor device of high quality can be manufactured is done so.

[0056] Moreover, in this invention, since the process of the conventional technique which requires the time amount of attaching a bump for every electrode of a semiconductor device is lost, it bundles up for every semiconductor device, it bundles up for every wafer further and inter-electrode junction is carried out, the effectiveness that productivity can be improved very greatly is done so.

[0057] Moreover, by using the insulating material which has the middle coefficient of thermal expansion of the coefficient of thermal expansion of a semiconductor device, and the coefficient of thermal expansion of the circuit board in the insulating material to be used, the thermal stress generated according to the difference of thermal expansion is eased, and the effectiveness that dependability can be improved is done so.

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**DESCRIPTION OF DRAWINGS**

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**[Brief Description of the Drawings]**

**[Drawing 1]** It is the sectional side elevation showing the configuration of the 1st example of the semiconductor device of this invention.

**[Drawing 2]** It is the top view showing the configuration of the 1st example of the semiconductor device of this invention.

**[Drawing 3]** It is the sectional side elevation showing the configuration of the 2nd example of the semiconductor device of this invention.

**[Drawing 4]** It is process drawing showing one example of the manufacture approach of the semiconductor device of this invention.

**[Drawing 5]** It is drawing which compares the process of this invention and the conventional example.

**[Drawing 6]** It is the sectional side elevation showing the configuration and operation of a semiconductor device of the 1st conventional example.

**[Drawing 7]** It is the sectional side elevation showing the configuration and operation of a semiconductor device of the 1st conventional example.

**[Drawing 8]** It is the sectional side elevation showing the configuration of the semiconductor device of the 2nd conventional example.

**[Description of Notations]**

1 Semiconductor Device

1a Semiconductor device

2 Semiconductor Device

4 Component Electrode

.4a Through tube  
17 Mask  
18 Exposure  
151 1st Insulating Layer  
151a The 1st insulating layer  
152 2nd Insulating Layer  
152a The 2nd insulating layer  
153 3rd Insulating Layer  
161 1st Wiring  
161a The 1st connection electrode  
161b Through tube  
162 2nd Wiring  
171 External Electrode  
171a Through tube

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[Translation done.]

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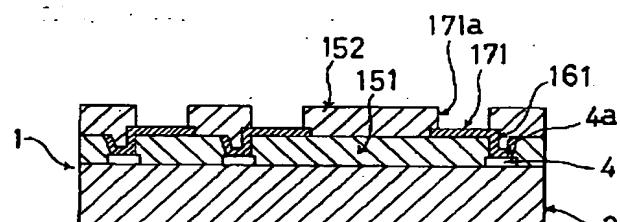
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(54)【発明の名称】 半導体装置とその製造方法

(57)【要約】

【目的】 半導体素子の素子電極数が多くなり、半導体素子の素子電極が小さくなり、電極ピッチが狭くなってしまい、高品質の製品を生産性良く製造できる半導体装置の提供。

【構成】 集積回路が形成され複数の素子電極4を有する半導体素子2と、前記半導体素子2の表面に形成された第1絶縁層151と、前記第1絶縁層151の上に形成された複数の外部電極171と、前記外部電極171と前記素子電極4とを電気的に接続する第1配線161とからなる第1導電層161、171とを有する。



1.....半導体装置  
2.....半導体素子  
4.....素子電極  
4 a.....貫通孔  
151.....第1絶縁層  
152.....第2絶縁層  
161.....第1配線  
171.....外部電極  
171 a.....貫通孔

(2)

2

## 【特許請求の範囲】

【請求項 1】 集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第1絶縁層と、前記第1絶縁層の上に形成された複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第1配線とからなる第1導電層とを有することを特徴とする半導体装置。

【請求項 2】 集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第1絶縁層と、前記第1絶縁層の上に形成され前記素子電極と電気的に接続された第1配線からなる第1導電層と、前記第1導電層の上に形成された第2絶縁層と、前記第2絶縁層の上に形成された複数の外部電極と、前記外部電極と前記第1配線または前記素子電極とを電気的に接続する第2配線とからなる第2導電層とを有することを特徴とする半導体装置。

【請求項 3】 半導体素子の表面に絶縁層と導電層とが繰り返し形成された多層配線構造を有し、前記多層配線構造を介して前記半導体素子の素子電極と電気的に接続された外部電極が最表面に形成されている請求項 2 に記載の半導体装置。

【請求項 4】 絶縁層の絶縁材料の熱膨張係数は、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の値である請求項 1、2 又は 3 に記載の半導体装置。

【請求項 5】 絶縁層の絶縁材料は感光性のエポキシ樹脂である請求項 1、2、3 又は 4 に記載の半導体装置。

【請求項 6】 集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第1絶縁層を設ける第1絶縁層形成工程と、前記第1絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第1配線とからなる第1導電層を設ける第1導電層形成工程とを有することを特徴とする半導体装置の製造方法。

【請求項 7】 集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第1絶縁層を設ける第1絶縁層形成工程と、前記第1絶縁層の上に導電性材料による導電層を形成し、整形して前記素子電極に接続する第1配線を有する第1導電層を設ける第1導電層形成工程と、前記第1導電層の上に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記第1配線に対する貫通孔を有する第2絶縁層を設ける第2絶縁層形成工程と、前記第2絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記第1配線または前記素子電極とを電気的に接続する第2配線とからなる第2導電層を設ける第2導電層形成工程とを有することを特徴とする半導体装置

## の製造方法。

【請求項 8】 半導体素子の表面に絶縁層形成工程と導電層形成工程とを繰り返して、多層配線構造を設け、前記多層配線構造を介して半導体素子の素子電極と電気的に接続される外部電極を最表面に設ける請求項 7 に記載の半導体装置の製造方法。

【請求項 9】 ウエハーの状態の複数の半導体素子に、絶縁層形成工程と導電層形成工程とを施す請求項 6、7 又は 8 に記載の半導体装置の製造方法。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】 本発明は、半導体素子を半導体キャリアに高密度に実装した半導体装置とその製造方法に関するものである。

## 【0002】

【従来の技術】 回路基板に高密度に実装する従来の半導体装置を図 5～図 8 に基づいて説明する。

【0003】 従来から、半導体素子 2 を回路基板 12 に実装する場合、図 6 に示すように、半導体素子 2 を、一旦、半導体キャリア 3 に接続して半導体装置 1 とした後に、回路基板 12 に接続している。これには、次の 2 つの理由がある。

【0004】 第 1 の理由は、ペア半導体素子のままで、傷が付き易くて実装前に検査ができない。従って、実装前に検査が行えるようにし、且つ、湿度による特性劣化を防ぐために、半導体素子 2 を半導体キャリア 3 に装着し、周辺をエポキシ系樹脂の封止剤 7 で充填被覆している。

【0005】 第 2 の理由は、ペア半導体素子は、構成上、素子電極位置がペア半導体素子の周辺部に偏りスペースが限られ、スペースが限られたこれらの素子電極 4 は、小さくて電極間距離が狭い。そのため、前記素子電極 4 を回路基板 12 の基板電極 11 に直接に接続するのが困難である。

【0006】 この接続を容易にするために、片面の素子側電極 6 の配置が半導体素子 2 の素子電極 4 への接続に適し、反対面の基板側電極 8 の配置が回路基板 12 の基板電極 11 への接続に適した半導体キャリア 3 の前記片面に、半導体素子 2 を接続し、前記の理由で、その周辺をエポキシ系樹脂の封止剤 7 で充填被覆している。

【0007】 従って、第 1 従来例では、図 6 において、半導体装置 1 は、半導体素子 2 の素子電極 4 を、その上に金のバンブ 5 を設けクリーム半田または導電性接着剤によって、半導体キャリア 3 の素子側電極 6 に接続し、接続した半導体素子 2 と半導体キャリア 3 間の隙間および接続した半導体素子 2 の周辺部をエポキシ系樹脂の封止剤 7 で充填被覆したものである。そして、前記素子側電極 6 と前記基板側電極 8 との間は電気的に接続されている。

【0008】 半導体装置 1 を回路基板 12 に接続する場

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合には、先ず図6に示すように、半導体キャリア3の前記基板側電極8にバンプ9を設け、回路基板12の基板電極11にクリーム半田13を印刷する。

【0009】次いで、図7に示すように、半導体装置1の基板側電極8を、回路基板12の基板電極11上に位置決めして載置し、加熱して前記塗布されたクリーム半田13を溶融・硬化して、基板側電極8を基板電極11に接続する。

【0010】次に、第2従来例を図8に基づいて説明する。

【0011】図8において、半導体装置1は、半導体素子2の複数の素子電極4の上に金のバンプ5を形成し、前記金のバンプ5を導電性接着剤5aによってポリイミドフィルム14上に形成された素子側電極6に接続し、半導体素子2とポリイミドフィルム14との間隙にはエポキシ樹脂の封止剤7が充填されている。そして、素子側電極6にバンプ9を設け、これを回路基板の電極に接続する。図8は断面を示すものであるが、実際には、半導体素子2の周辺部に偏っている多数の素子電極4が紙面に垂直方向に密に配置されており、素子側電極6は、半導体素子2の中央部の広いスペースに格子状に配置されている。

【0012】

【発明が解決しようとする課題】しかし、上記の従来例の構成では、半導体素子のウエハーから半導体装置として出荷するまでの工程が、図5に示すように、分割工程で、半導体素子のウエハーを一つ一つの半導体素子に分割し、バンプ形成工程で、一つ一つの半導体素子に対してその素子電極の数だけのバンプ形成を繰り返し、位置決め・接合工程で、バンプ形成が終了した半導体素子を、半導体キャリアに一つ一つ位置決め・接合する必要がある。

【0013】従って、最近のように半導体素子の素子電極の数が多くなると生産工程に非常に時間がかかるという問題点がある。

【0014】又図6、図7に示す封止剤7の硬化工程にも長時間を要するという問題点がある。

【0015】又、半導体キャリア3に求められる特性として、その平坦度は、電極接合強度の信頼性を維持するために、反り量が10μm以下、基板側電極の大きさは100μm×100μm以上であり、反り量が10μmを越えると電極接合不良が発生し、基板側電極の面積が不足したり、ピッチが狭くなり過ぎると、高品質の製造が困難になり、ブリッジ等の不良が発生するという問題点がある。

【0016】本発明は、上記の問題点を解決し、半導体素子の素子電極数が多くなり、半導体素子の素子電極が小さくなり、電極ピッチが狭くなってしまっても、高品質の製品を生産性良く製造できる半導体装置とその製造方法を提供することを課題とする。

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【0017】

【課題を解決するための手段】本願第1発明の半導体装置は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第1絶縁層と、前記第1絶縁層の上に形成された複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第1配線とからなる第1導電層とを有することを特徴とする。

【0018】本願第2発明の半導体装置は、上記の課題

10 を解決するために、集積回路が形成され複数の素子電極を有する半導体素子と、前記半導体素子の表面に形成された第1絶縁層と、前記第1絶縁層の上に形成された複数の素子電極と電気的に接続された第1配線からなる第1導電層と、前記第1導電層の上に形成された第2絶縁層と、前記第2絶縁層の上に形成された複数の外部電極と、前記外部電極と前記第1配線または前記素子電極とを電気的に接続する第2配線とからなる第2導電層とを有することを特徴とする。

【0019】又、本願第2発明の半導体装置は、上記の

20 課題を解決するために、半導体素子の表面に絶縁層と導電層とが繰り返し形成された多層配線構造を有し、前記多層配線構造を介して前記半導体素子の素子電極と電気的に接続された外部電極が最表面に形成されていることが好適である。

【0020】又、本願第1、第2又は第3発明の半導体装置は、上記の課題を解決するために、絶縁層の絶縁材料の熱膨張係数は、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の値であることが好適である。

【0021】又、本願第1、第2、第3又は第4発明の半導体装置は、上記の課題を解決するために、絶縁層の絶縁材料は感光性のエポキシ樹脂であることが好適である。

【0022】本願第3発明の半導体装置の製造方法は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第1絶縁層を設ける第1絶縁層形成工程と、前記第1絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記素子電極とを電気的に接続する第1配線とからなる第1導電層を設ける第1導電層形成工程とを有することを特徴とする。

【0023】本願第4発明の半導体装置の製造方法は、上記の課題を解決するために、集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第1絶縁層を設ける第1絶縁層形成工程と、前記第1絶縁層の上に導電性材料による導電層を形成し、整形して前記素子電極とを電気的に接続する第1配線とからなる第1導電層を設ける第1導電層形成工程とを有することを特徴とする。

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導電層形成工程と、前記第1導電層の上に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記第1配線に対する貫通孔を有する第2絶縁層を設ける第2絶縁層形成工程と、前記第2絶縁層の上に導電性材料による導電層を形成し、整形して複数の外部電極と、前記外部電極と前記第1配線または前記素子電極とを電気的に接続する第2配線とからなる第2導電層を設ける第2導電層形成工程とを有することを特徴とする。

【0024】又、本願第4発明の半導体装置の製造方法は、上記の課題を解決するために、半導体素子の表面に絶縁層形成工程と導電層形成工程とを繰り返して多層配線構造を設け、最表面に前記多層配線構造を介して半導体素子の素子電極と電気的に接続される外部電極を設けることが好適である。

【0025】又、本願第3又は第4発明の半導体装置の製造方法は、上記の課題を解決するために、ウエハーの状態の複数の半導体素子に、絶縁層形成工程と導電層形成工程とを施すことが好適である。

【0026】

【作用】本願発明の半導体装置と、本願発明の半導体装置の製造方法とは、集積回路が形成され複数の素子電極を有する半導体素子の表面に感光性絶縁材料による絶縁層を形成し、マスクを使用して露光し、現像して、前記素子電極に対する貫通孔を有する第1絶縁層を設ける第1絶縁層形成工程と、前記第1絶縁層の上に導電性材料による導電層を形成し、整形して前記素子電極に接続する第1配線を有する第1導電層を設ける第1導電層形成工程との組合せによるものであり、これらの工程は半導体素子の製造技術の実績を利用してできるので、超微細化される半導体素子の素子電極やそのピッチに対応して、高品質な半導体装置を得ることができる。

【0027】又、半導体素子の各素子電極毎にバンプを取り付けるという時間がかかる従来技術の工程が無くなり、各半導体素子毎に一括して、更に、各ウエハーごとに一括して素子電極と外部電極間の電極接合を行うので、生産性を極めて大きく向上できる。

【0028】又、使用する絶縁材料に、半導体素子の熱膨張係数と回路基板の熱膨張係数との間の熱膨張係数を持つ絶縁材料を使用することによって、熱膨張の差によって発生する熱応力を緩和し信頼性を向上できる。

【0029】

【実施例】本発明の半導体装置の第1実施例を図1、図2に基づいて説明する。

【0030】図1、図2において、本実施例の半導体装置1の構造は、複数の素子電極4を有する半導体素子2の上に第1絶縁層151が形成されており、素子電極4の上には、貫通孔4aが設けられている。第1絶縁層151の上には第1配線161と第1外部電極171とが設けられ、第1配線161は第1外部電極171と素子電極4を接続する。

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極4とを接続している。第1絶縁層151と第1配線161と第1外部電極171との上には、第2絶縁層152が設けられ、第1外部電極171の上には貫通孔171aが開けられている。この第1外部電極171が本実施例の半導体素子1の外部電極になる。

【0031】そして、素子電極4は、図2に示すように、半導体素子2の構成によって、半導体素子2の周辺部に偏って配置されているので、半導体素子2が小型化され、且つ、素子電極4の数が多くなると、素子電極4の面積が小さくなり、電極間ピッチが狭くなるが、第1外部電極171は、半導体素子2の中央部の広いスペースに配置され、形、面積、配置の制限が少なく、図2に示すように、回路基板の基板電極に接続し易い配置に、例えば、格子状等の配置に自由に設計できる。

【0032】本発明の半導体装置の第2実施例を図3に基づいて説明する。

【0033】図3において、本実施例の半導体装置1'aの構造は、第1実施例の構造を多層構造にしたものである。

【0034】複数の素子電極4を有する半導体素子2上に第1絶縁層151が形成されており、素子電極4の上には、貫通孔4aが設けられている。

【0035】第1絶縁層151の上には第1配線161と第1接続電極161aとが設けられ、第1配線161は素子電極4と第1接続電極161aとに接続している。

【0036】第1絶縁層151と第1配線161と第1接続電極161aとの上には、第2絶縁層152が設けられ、第1接続電極161aの上には貫通孔161bが設けられている。

【0037】第2絶縁層152の上には第2配線162と第2外部電極172とが設けられ、第2配線162は第1接続電極161aに接続している。

【0038】第2絶縁層152と第2配線162と第2外部電極172との上には、第3絶縁層153が設けられ、第2外部電極172の上には貫通孔172aが設けられている。

【0039】上記の多層構造は、2層に限らず、何層でも可能であり、これらの層の配線部に、抵抗、容量等の回路素子の付加を設計することができる。

【0040】本発明の半導体装置の製造方法を図4、図5に基づいて説明する。

【0041】図4において、先ず、第1の絶縁層形成工程で、素子電極4を有する半導体素子2の表面に感光性絶縁材料で第1の絶縁層151aを形成する。感光性絶縁材料はエポキシ系樹脂であることが好ましい。第1の絶縁層151aの形成は、液状のものを印刷しても良く、フィルム状のものを付着させても良い。

【0042】次に、露光工程で、所定パターンの光が通過するように形成されたマスク17を使用して露光18

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する。

【0043】次に、現像工程で、現像することによつて、素子電極4の上に貫通孔4aを設け、第1絶縁層151を形成する。

【0044】次に、第1の導電性材料層形成工程で、前記の第1絶縁層151と貫通孔4aと素子電極4との上に、第1の導電性材料層171cを形成する。この第1の導電性材料層171cの形成には、薄膜を形成することができ、ファインパターンを形成できるものであれば、メッキ、スパッタリング、蒸着等の各種の加工方法を自由に選択できる。

【0045】次に、整形工程で、前記第1導電性材料層171cから、必要な部分を残して、エッチングを行い、第1配線161と外部電極171とを形成する。勿論、整形方法も自由に選択できる。

【0046】次に、第2の絶縁層形成工程で、第1絶縁層151と第1配線161と外部電極171との表面に感光性絶縁材料で第2の絶縁層152aを形成する。感光性絶縁材料はエポキシ系樹脂であることが好ましい。第2の絶縁層151aの形成は、液状のものを印刷しても良く、フィルム状のものを付着させても良い。

【0047】次に、露光・現像工程で、露光し、現像することによって、外部電極171の上に貫通孔171aを設け、第2絶縁層152を形成する。

【0048】図4において、複数の外部電極171の相互間隔が狭くなっているように見えるが、実際には、例えば、図2に示すように、紙面に垂直方向に離れている格子状の配置である。

【0049】場合によつては、第n配線層形成工程、第n絶縁層形成工程までを繰り返して多層構造にする。その際に、各配線層に抵抗、容量等の素子を付加できる。そして、上記に使用する絶縁材料は、表1に示すように、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の熱膨張係数を持つ材料が好ましい。

#### 【0050】

【表1】

素 材	熱膨張係数 (10 <sup>-6</sup> / °C)
半導体素子	2.4
絶縁層	3~6
回路基板 (アルミナ基板)	7

【0051】尚、実施例の説明に使用した図4では、配線層形成工程と絶縁層形成工程とを、半導体素子ウエハーを分割した後に行うような図になっているが、第n配線層形成工程、第n絶縁層形成工程を、半導体素子ウエハーの分割前の状態で、そのウエハー全体の半導体素子を一括して処理できるので、作業効率が極めて大きく向

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上する。

【0052】又、配線層形成工程と絶縁層形成工程とは、半導体素子の製造工程と同様の工程の繰り返しであるので、これらの加工精度は、半導体素子の製造実績と同等のものが可能であるから、超微細化される電極やそのピッチに対応して、高品質の半導体装置の製造が可能である。

【0053】図5に基づいて、本発明と従来例との工程を比較する。

【0054】図5において、右側の従来例は前記の説明の通りであるが、左側の本発明の場合には、第n配線層形成工程と第n絶縁層形成工程とを、半導体素子ウエハーの分割前の状態で、そのウエハー全体の半導体素子を一括して処理できるので、従来例で、半導体素子ウエハーを分割してから、半導体素子の一枚一枚毎に、それらの各電極毎に、バンプを形成するのに比較して、作業効率が極めて向上する。

#### 【0055】

【発明の効果】本発明の半導体装置とその製造方法では、配線層形成工程と絶縁層形成工程とが共に、半導体素子の製造工程と同様の工程の繰り返しであるので、超微細化される半導体素子の電極やそのピッチに対応することができ、高品質の半導体装置を製造できるという効果を奏する。

【0056】又、本発明では、半導体素子の各電極毎にバンプを取り付けるという時間がかかる従来技術の工程が無くなり、各半導体素子毎に一括して、更に、各ウエハーごとに一括して電極間接合するので、生産性を極めて大きく向上できるという効果を奏する。

【0057】又、使用する絶縁材料に、半導体素子の熱膨張係数と回路基板の熱膨張係数との中間の熱膨張係数を持つ絶縁材料を使用することによって、熱膨張の差によって発生する熱応力を緩和し信頼性を向上できるという効果を奏する。

#### 【図面の簡単な説明】

【図1】本発明の半導体装置の第1実施例の構成を示す側断面図である。

【図2】本発明の半導体装置の第1実施例の構成を示す平面図である。

【図3】本発明の半導体装置の第2実施例の構成を示す側断面図である。

【図4】本発明の半導体装置の製造方法の一実施例を示す工程図である。

【図5】本発明と従来例との工程を比較する図である。

【図6】第1従来例の半導体装置の構成と使用方法とを示す側断面図である。

【図7】第1従来例の半導体装置の構成と使用方法とを示す側断面図である。

【図8】第2従来例の半導体装置の構成を示す側断面図である。

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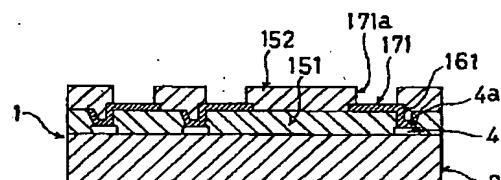
## 【符号の説明】

1 半導体装置  
 1 a 半導体装置  
 2 半導体素子  
 4 素子電極  
 4 a 貫通孔  
 17 マスク  
 18 露光  
 151 第1絶縁層  
 151 a 第1の絶縁層

10

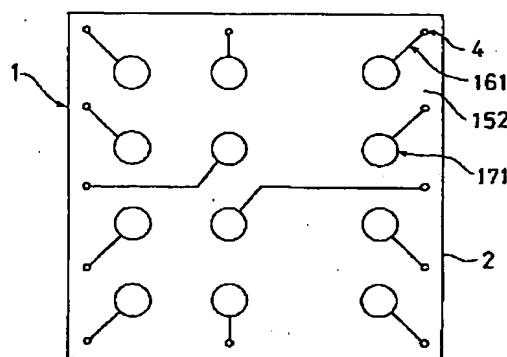
152 第2絶縁層  
 152 a 第2の絶縁層  
 153 第3絶縁層  
 161 第1配線  
 161 a 第1接続電極  
 161 b 貫通孔  
 162 第2配線  
 171 外部電極  
 171 a 貫通孔

【図1】

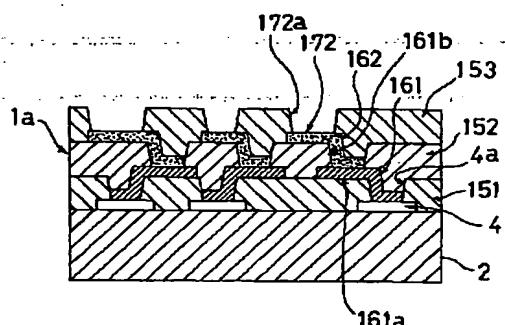


1 半導体装置  
 2 半導体素子  
 4 素子電極  
 4 a 貫通孔  
 151 第1絶縁層  
 152 第2絶縁層  
 161 第1配線  
 171 外部電極  
 171 a 貫通孔

【図2】

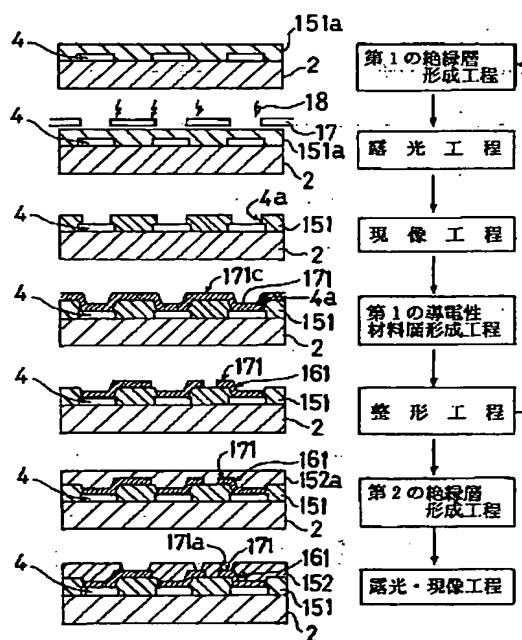


【図3】



1 a 半導体装置  
 153 第3絶縁層  
 161 a 第1接続電極  
 161 b 貫通孔  
 162 第2配線  
 172 外部電極  
 172 a 貫通孔

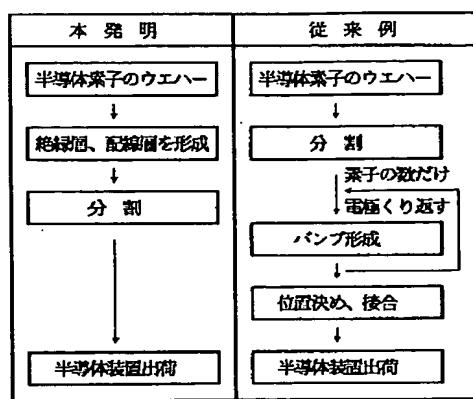
【図4】



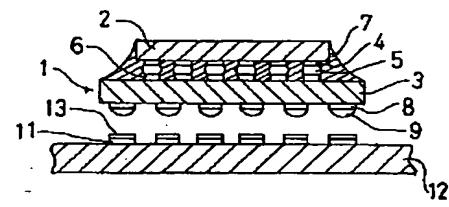
17 マスク  
 18 露光  
 151 a 第1の絶縁層  
 152 a 第2の絶縁層  
 171 c 第1の導電性材料層

(7)

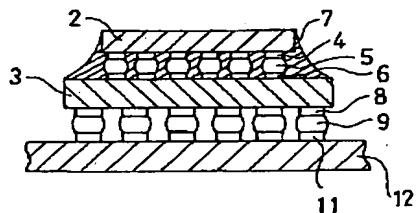
【図5】



【図6】



【図7】



【図8】

